



TECHNICAL SKILLS – ROAD MAP

May 2010

1°) Purpose

This non-contractual document is intended to document our current knowledge base. The document indicates our current capabilities under the terms “*Classical*” (traditional production techniques) or “*Technical*” (advanced production techniques). It also contains the term “*Special*” (very low volumes, particularly difficult to realise), where the manufacturing process is not fully qualified. It equally assumes that these processes will be qualified, and is shown in our roadmap under “Year + 1”.

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2°) Overview and Roadmap

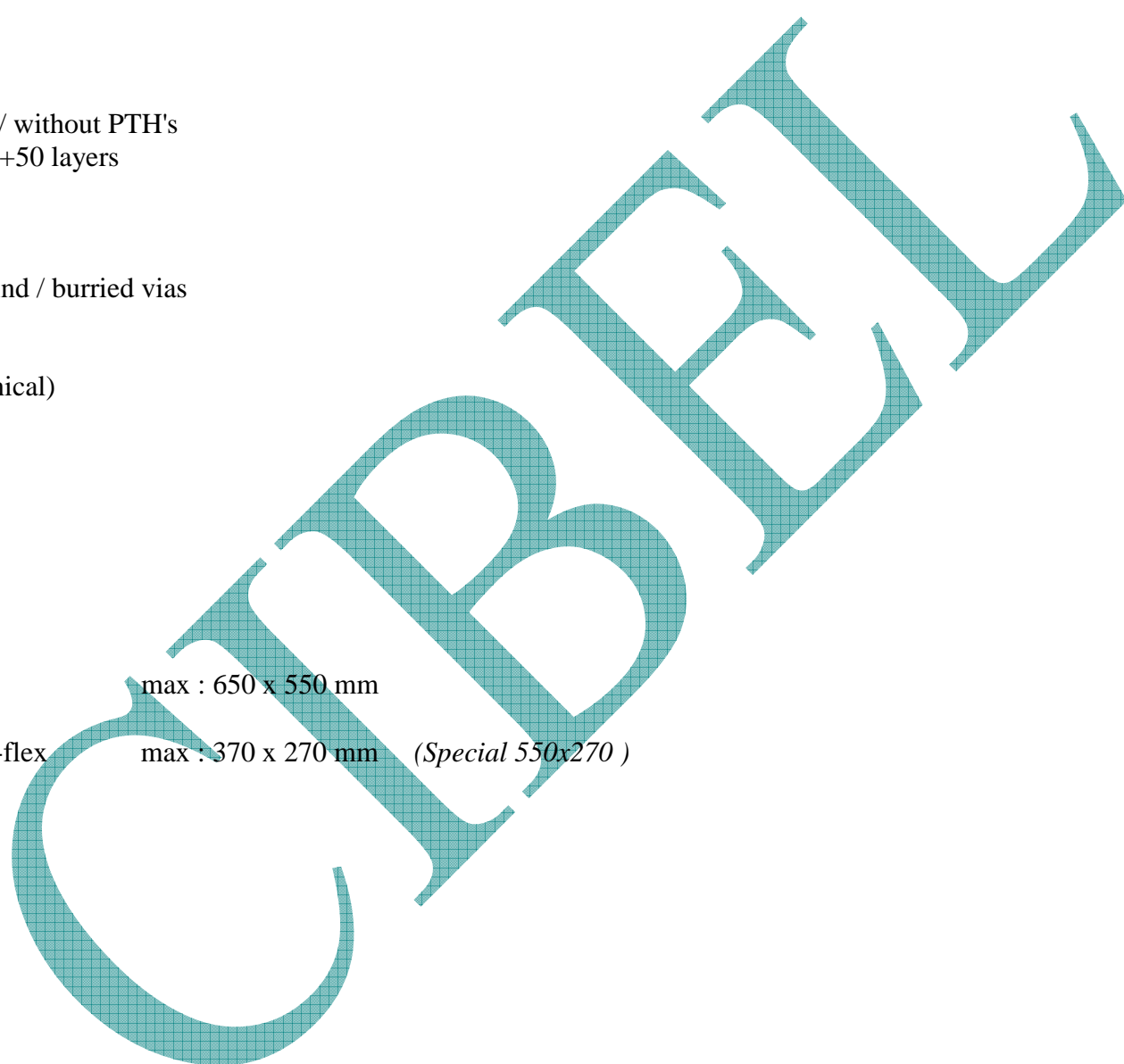
	<i>See Chapter</i>	<i>2010</i>			<i>2011...</i>	
		<i>Classical</i>	<i>Technical</i>	<i>Special</i>	<i>Classical</i>	<i>Technical</i>
Max rigid PCB dimensions	4	650x550mm	650x550mm	-	650x550mm	650x550mm
Max flexible PCB dimensions	4	370x270mm	550x270mm	-	550x270mm	600x500mm
Max PCB thickness	6, 9.1, 9.2	3.2mm	6.0mm	6.5	3.2mm	6.5mm
Max layers count	-	24	+40	+50	40	+50
Min "inter-layer" thickness	9.3	0.10mm	0.045mm	0.045mm	0.080mm	0.045mm
Min drilled hole size	9.1, 9.2, 9.3	0.150mm	0.100mm	0.075mm	0.100mm	0.060mm
Tolerance on Z axis drilled holes	-	+/-0.075mm	+/-0.06mm	+/-0.04mm	+/-0.06mm	+/-0.05mm
“ Back drill “	9.3.1.1	-	-	diam +0.20mm	-	diam +0.15mm
PTH:Cu Aspect Ratio	9.1, 9.2, 9.3	10/1	See chapter 9.1/9.2	-	See chapter 9.1/9.2	-
Z axis drilling Aspect Ratio	9.3	1/1	See chapt 9.1/9.2	-	See chapt 9.1/9.2	-
Vias filling	-	pre-preg or plugging paste	pre-preg or plugging-paste	pre-preg or plugging-paste	pre-preg or plugging paste	pre-preg or plugging-paste
Min. Line space (between conductor and insulating materiel)	8	120µm	See Chapter 8	45µm	100µm	See Chapter 8
Min “drilled hole / copper” distance	9.4	0.150mm	0.100mm	0.080mm	0.150mm	0.080mm
Impedance control	-	+/-10%	+/-5%	+/-5%	+/-10%	+/-5%
Max sequential lamination/drilling	10	3	5	8	4	6

3°) Types of PCB's

- Single layer
- Double layers with / without PTH's
- Multilayers 3 up to +50 layers
- Flexible
- Flex-rigid
- Hi- frequency
- Multilayers with blind / burried vias
- Impedance control
- Heat sinks
- Micro-vias (mechanical)
- Press-fit PCB's
- Mixed substrates

4°) Board size

- Rigid PCB's max : 650 x 550 mm
- Flexible / Rigid-flex max : 370 x 270 mm (*Special 550x270*)



5°) Currently used substrates :

- FR4
- FR4 HTg
- Polyimides (including Kapton)
- BT Epoxy
- Substrates « Hyper » (of which RO 3..., RO 4..., Cuclad..., Diclاد..., TMM... etc...)

6°) PCB thickness limits

- Max rigid : 5.5 mm (*Special 6.5mm*)
- Min rigid : 100 µm (*Special 75µm*)
- Min flexible : 50 µm (*Special 25µm*)
- "inter-layer" min : +/-50 µm

7°) Copper base layer thickness (int or ext)

- minimum basis copper thickness :9µm
- maximum basis copper thickness : ...210µm (*Special 400µm*)

8°) Minimum space between tracks, and their tolerances (iT) relative to copper base layer thickness

8.1 Inverse Copper etching (PCB external layers with PTH)

A. Copper base thickness (μm)	Classical Products		<i>Technical Products</i>		<i>Special Products</i>	
	Min. spacing between tracks (μm)	iT	Min. spacing between tracks (μm)	<i>iT</i>	Min. spacing between tracks (μm)	<i>iT</i>
5	-	-	-	-	45	10
9/12	-	-	70	20	50	15
17,5	12	30	90	25	70	20
35	150	40	120	35	90	25
70	210	60	150	45	110	30
105	310	100	200	70	150	50
210	500	150	320	130	250	100

8.2 « Direct » etching (external layers, PCB without PTH)

B. Copper base thickness (µm)	Classical Products		<i>Technical Products</i>		<i>Special Products</i>	
	Min. spacing between tracks (µm)	iT	Min. spacing between tracks (µm)	<i>iT</i>	Min. spacing between tracks (µm)	<i>iT</i>
5	-	-	-	-	40	10
9/12	-	-	60	10	50	15
17,5	110	20	75	15	60	15
35	135	35	105	30	80	25
70	180	50	140	40	110	30
105	250	100	180	60	150	50
210	500	150	320	130	250	100

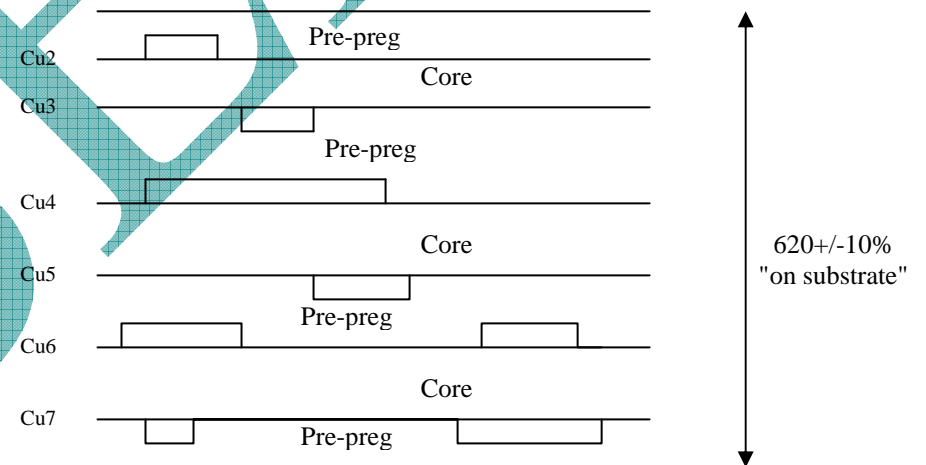
* iT = tolerance variation (Δ Min/Max) : 0/-x iT for **tracks**
 0/+x iT for the **spaces**
 or +/- 1/2x iT for both **tracks and spaces**

9°) Drilling

9.1 Mechanical "Through" holes, classical stack up (core substrate FR4 /FR4 HTG e=100µm +/-10% thick, pre-preg e=50µm +/-10% thick)

Layer count Cu 17.5µm	Min total thickness "on substrate" +/-10% (FR4, FR4 HTg) in µm	Ø min drilled / "platable" in mm	Aspect Ratio e / Ø
2	135	0.050	2.7
4	260	0.080	3.3
6	440	0.080	5.5
8	620	0.100	6.2
10	800	0.100	8
12	980	0.125	7.9
14	1160	0.125	9.3
16	1340	0.150	8.9
18	1520	0.150	10.1
20	1700	0.150	11.3
22	1880	0.200	9.4
24	2060	0.200	10.3
26	2240	0.250	9
28	2420	0.250	9.7

8 layer example

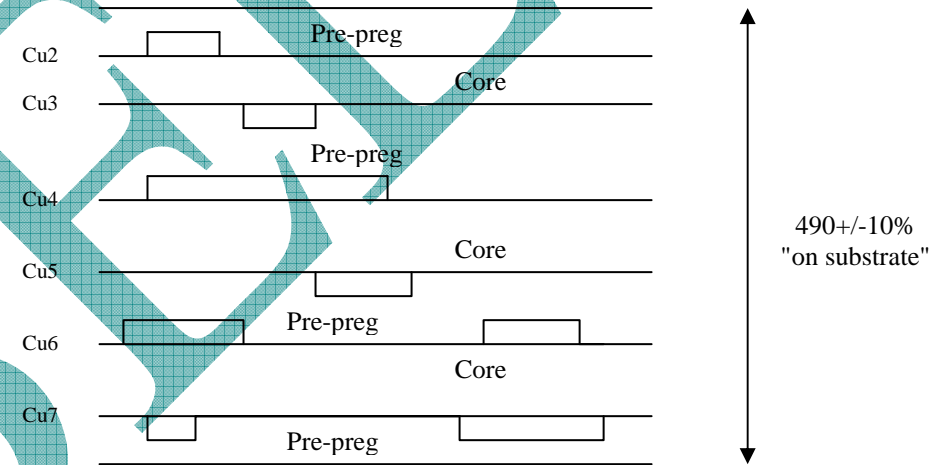


Note : from e ≥ 2200, aspect ratio e/Ø may be greater than 11
 (e=3200 , Ø 0.25 Ratio = 12.8 ; e= 4000, Ø 0.30 Ratio = 13.3) if N copper-clad Layers ≤ 20

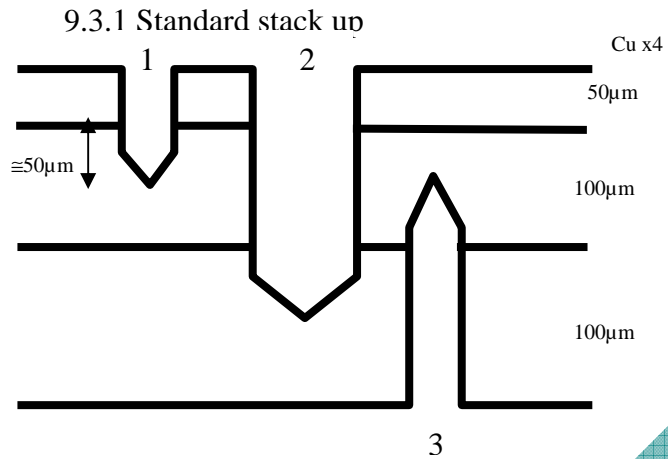
9.2 Mechanical "Through"holes, "Special" Stack up (all dielectrics 50µm +/-10%)

Layer count Cu 17.5µm	Min total thickness "on substrate" +/-10% (FR4, FR4 HTg) in µm	Ø min drilled / "platable" in mm	Aspect Ratio e / Ø
2	85	0.050	1.7
3	160	0.050	3.2
4	225	0.080	2.8
5	290	0.080	3.6
6	360	0.080	4.5
7	425	0.080	5.3
8	490	0.080	6.1
9	560	0.100	5.6
10	625	0.100	6.2
11	690	0.100	6.9
12	760	0.100	7.6

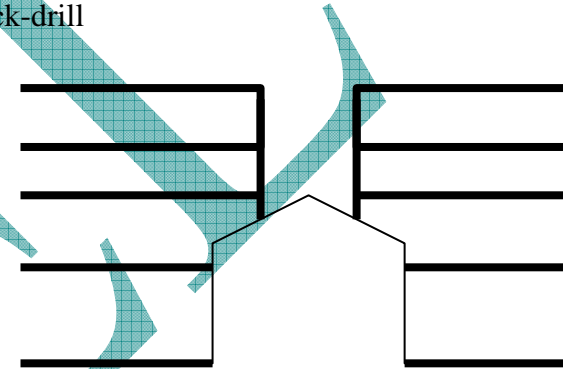
8 layers example



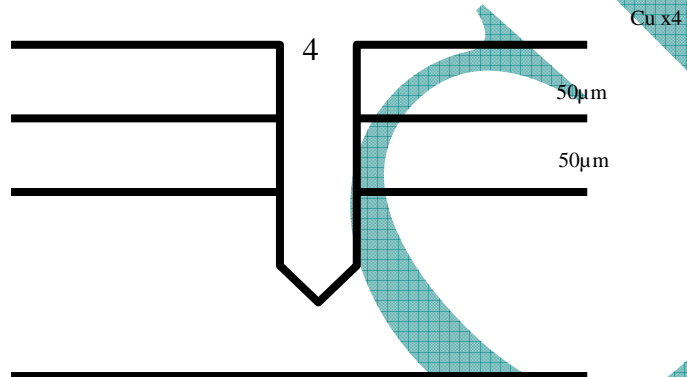
9.3 Z axis controlled thickness drilling



9.3.1.1 Back-drill



9.3.2 Special stack up



Configuration	Thickness	STANDARD		ADVANCED	
		Ø min drilled	Ratio	Ø min drilled	Ratio
1	130µm	125µm	1.05	100µm	1.30
2	185µm	175µm	0.95	150µm	1.25
3	250µm	250µm	1	225µm	1.10
4	190µm	200µm	0.95	175µm	1.10

9.3.3 Other cases (blind holes)

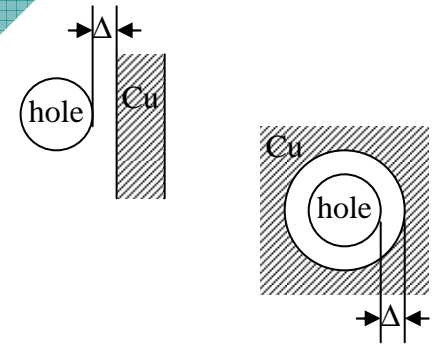
- $200\mu\text{m} > e \geq 700\mu\text{m}$ ratio $e / \varnothing = 1$
- $800\mu\text{m} > e \geq 1600\mu\text{m}$ ratio $e / \varnothing = 1.2$

9.4 Minimum space “drilled hole / copper entity” (Δ)

9.4.1 General values

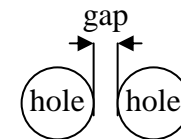
- $\Delta \geq 12.5\mu\text{m} \times N$ layers "from the same lamination sequence"
- Δ mini recommended : $120\mu\text{m}$ - Conductive Anodic Filament (CAF) risk
- Absolute min Δ : $80\mu\text{m}$ (with restrictions concerning duration and using conditions : CAF !!)

9.4.2 Δ also depends on the PCB's size (contact us)



9.5 minimum space “PTH/PTH” (drilled hole/ drilled hole gap)

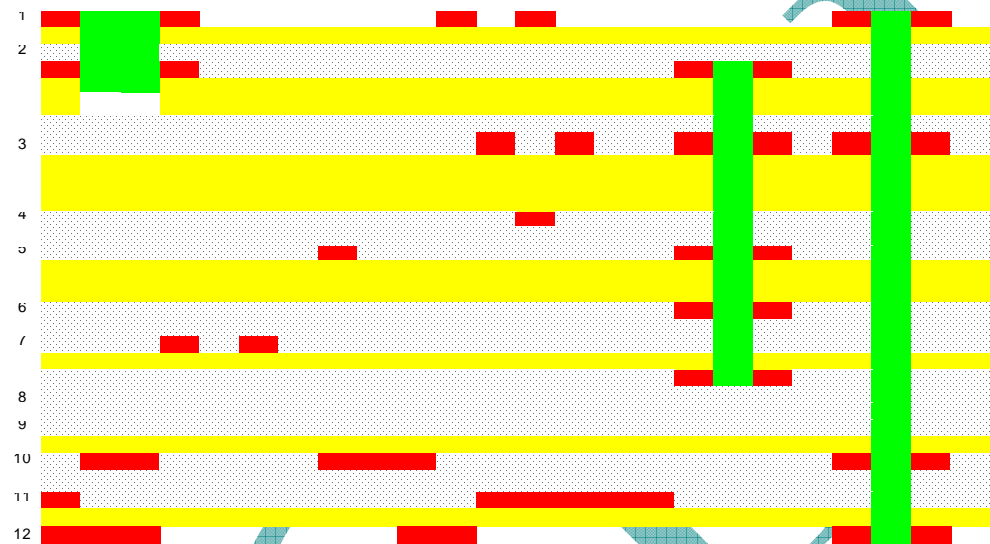
- Min Space recommended : $200\mu\text{m}$ (CAF!)
- Absolute min Δ : $100\mu\text{m}$ (with restrictions concerning duration and using conditions : CAF !!)



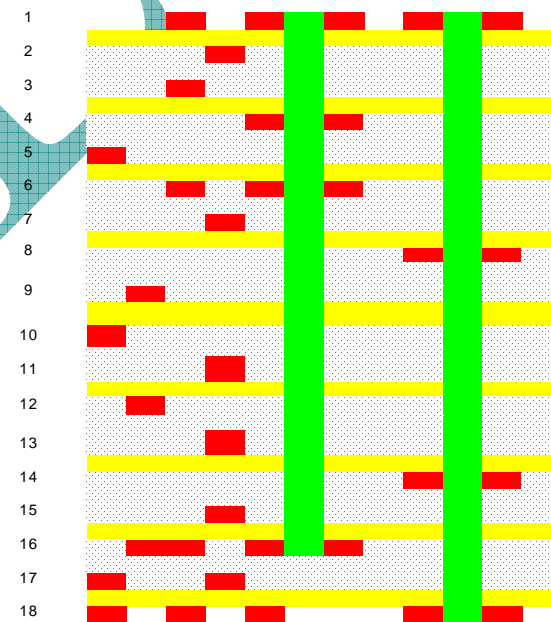
9.6 LASER drilling

Outsourced

10°) Stack –up examples



ML12, 2 laminations, 3 drilling (with one Z axis controlled drilling)



ML18, 2 laminations, 2 drilling

core
preg

11°) Finishes.

- COPPER : up to 50µm
- TIN-LEAD (non ROHS !) :
Sn 63%/Pb 37%
 - electrolytic (reflowed or not) : 10 to 20µm
 - HAL : 3 to 50µm (depending on design)
- ELECTROLYTIC NICKEL/GOLD (Hard gold):
Ni : 3 to 25µm Au : 0.1µm to 1.5µm
- ELECTROLYTIC NICKEL/GOLD (Pure "Bonding" gold) :
Ni : 5 to 10µm Au : 1 to 3µm
- ELECTROLESS NICKEL/GOLD (ENIG)
Ni de 3 à 7 µm + Au < 0,1µm
- ELECTROLESS SILVER :
about 0.2µm deposited
- ELECTROLESS NICKEL :
Ni : 3 to 10 µm
- IMMERSION TIN :
+/- 1.3µm
- LEAD FREE HAL (SN100C) :
1 to 50µm (dependant on configuration)

12° MISCELLANEOUS

- SOLDER MASK : Photo imageable green color (other colors available)
- SOLDER MASK for flexible PCB's
- COVERLAY
- PHOTOIMAGEABLE COVERLAY
- LEGEND PRINTING : Ink-jet process (white) or screen-printing (other colors)
- IMPEDANCES : Calculation and control of the files by POLAR
Measurement made with Reflectometer POLAR INSTRUMENTS CITS 200
- ELECTRICAL TEST : 3 FLYING PROBE TEST SYSTEMS ATG type A2 et A3
Standard Value : 10V (up to 500V adjustable)
Insulation : >10MOhms
Continuity threshold < 10 Ohms
- AOI with CAMTECH ORION 604
- THICKNESS MEASUREMENT : - CAVIDERM (micro-ohmmeter)
 - Cross-sections
 - FISCHER (Fluorescence X)